UNITED STATES PATENT APPLICATION

for

A BIASING TECHNIQUE FOR A HIGH DENSITY SRAM

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A Biasing Technique For a High Density SRAM

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FIELD OF THE INVENTION

[0002]   The present invention relates to memory devices; more particularly, the present invention relates to static random access memories (SRAMs).

BACKGROUND

[0003]   Since the dawn of the electronic revolution in the 1970's, continuous technological advances in the computer industry have depended upon the ability to store and retrieve an ever-increasing amount of data quickly and inexpensively. Thus, the development of the semiconductor memory has played a major role in the advancement of the computer industry over the past few decades.

[0004]   In particular, with the growing demand for large-scale on-chip cache memory for high performance microprocessors, a high-density static

random access memories (SRAM) design becomes more significant.

Traditionally six transistor (6T) SRAM cells have been implemented for cache memory devices. However, the size of 6T SRAM cells have become undesirable.

As a result, four transistor (4T) SRAM cells have become more desirable because of smaller cell areas. Nonetheless, there is a problem with the design of 4T

SRAM cells since it is typically difficult to meet read stability requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005]   The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention. The drawings, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

[0006]   **Figure 1** is a block diagram of one embodiment of a computer system;

[0007]   **Figure 2** illustrates an exemplary four-transistor memory;

[0008]   **Figure 3** illustrates one embodiment of a four transistor memory cell with forward bias; and

[0009]   **Figure 4** illustrates one embodiment of a memory device.

DETAILED DESCRIPTION

[0010]   A biasing technique for static random access memories (SRAMs) implementing four transistor memory cells is described. According to one embodiment, the delivery of a forward bias voltage during a memory cell standby state enables an access and load transistor to maintain a storage value within the memory cell by helping to provide a leakage current from the access and load transistor. Moreover, the delivery of a reverse bias voltage during a memory cell read state enables an access and load transistor to prevent the memory cell from switching its value during the read.

[0011]   In the following description, numerous details are set forth. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

[0012]   Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0013]   **Figure 1** is a block diagram of one embodiment of a computer system 100. Computer 100 includes a processor 101 that processes data signals.

Processor 101 may be a complex instruction set computer (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a processor implementing a combination of instruction sets, or other processor device.

[0014]   In one embodiment, processor 101 is a processor in the Pentium® family of processors including the Pentium® II family and mobile Pentium® and Pentium® II processors available from Intel Corporation of Santa Clara, California. Alternatively, other processors may be used. **Figure 1** shows an example of a computer system 100 employing a single processor computer. However, one of ordinary skill in the art will appreciate that computer system 100 may be implemented using having multiple processors.

[0015]   Processor 101 is coupled to a processor bus 110. Processor bus 110 transmits data signals between processor 101 and other components in computer system 100. Computer system 100 also includes a memory 113. In one embodiment, memory 113 is a dynamic random access memory (DRAM) device. However, in other embodiments, memory 113 may be a static random access memory (SRAM) device, or other memory device.

[0016]   Memory 113 may store instructions and code represented by data signals that may be executed by processor 101. According to one embodiment, a cache memory 102 resides within processor 101 and stores data signals that are also stored in memory 113. Cache 102 speeds up memory accesses by processor 101 by taking advantage of its locality of access.

[0017]   In another embodiment, cache 102 resides external to processor 101.

Computer system 100 further comprises a bridge memory controller 111 coupled

to processor bus 110 and memory 113. Bridge/ memory controller 111 directs

data signals between processor 101, memory 113, and other components in

computer system 100 and bridges the data signals between processor bus 110

and memory 113.

[0018]   Typically, six transistor (6T) SRAM cells have been implemented

for cache memory devices. However, the size of 6T SRAM cells have become

undesirable. As a result, four transistor (4T) SRAM cells have become more

desirable because of smaller cell areas. **Figure 2** illustrates an exemplary

memory cell. The memory cell includes two PMOS transistors (P1 and P2) and

two NMOS transistors (N1 and N2). In addition, the memory cell includes

storage node 1 and storage node 2.

[0019]   The memory cell typically operates in three modes, STANDBY,

READ AND WRITE. While in the STANDBY mode, substantial off-state leakage

currents are provided from the PMOS transistors to the respective NMOS

transistors in order to maintain data storage at storage node 1 and storage node

2. Thus, the PMOS transistors are designed to be strong enough to provide the

necessary leakage current.

[0020]   However, if the PMOS transistors are too strong, the current

flowing through transistor P1 or transistor P2 during the READ mode can pull

nodes 1 and 2 up, thus flipping the memory cell. Consequently, the loss of the

memory state occurs. In order to prevent such an occurrence, transistor N1 typically has to be as least 1.5 times stronger than transistor P1 to ensure cell stability while in the READ mode. However, the increased size of transistor N1 results in a larger area for the memory cell.

[0021]   **Figure 3** illustrates one embodiment of a memory cell 300. Memory cell 300 includes PMOS transistors 310 and 320, and NMOS transistors 330 and 340. Transistors 310 and 320 serve as access and load transistors. The gate of transistor 310 is coupled to WORDLINE. WORDLINE is used to activate a row of cells 300 within a SRAM device (e.g., cache 102).

[0022]   The source of transistor 310 is coupled to one of two bit lines (BITLINE), while the drain is coupled to the drain of transistor 330 at storage node 1. The BITLINE is used to activate a column of cells within the SRAM device. The gate of transistor 320 is also coupled to WORDLINE. The source of transistor 320 is coupled to the other bit line (BITLINE#), and the drain is coupled to the drain of transistor 340 at storage node 2.

[0023]   Transistors 330 and 340 serve as the body of the SRAM device. The gate of transistor 330 is coupled to the drain of transistor 320 at storage node 2. As described above, the drain of transistor 330 is coupled to storage node 1, and the source is coupled to ground. The gate of transistor 340 is coupled to the drain of transistor 310 at storage node 1. Also, the drain of transistor 340 is coupled to node 2, and the source is coupled to ground.

[0024]   According to one embodiment, transistors 310 and 320 include a

body bias (Vb) that is received from a body control signal. In one embodiment, the body control signal is received from processor 101. However, in other embodiments, the body control signal may be received from memory controller 111. In a further embodiment, transistors 310 and 320 receive a forward body bias during the STANDBY mode and a reverse body bias during the READ mode, as described in further detail below.

[0025] While operating in the STANDBY mode, both bit lines and WORDLINE are at a high logic level (e.g., logic 1). Assuming that storage node 1 starts at a high logic level (e.g., logic 0) and storage node 2 starts at a low logic level, node 1 is driven to a low logic level and node 2 is driven high. As a result, a data value is being stored at node 2. The off-state leakage current from transistor 320 helps maintain a logic high value at storage node 2. During the STANDBY mode, the body control signal is received at transistors 310 and 320 as a forward bias.

[0026] Forward bias is a voltage supplied to transistors 310 and 320 that is less than Vcc. The forward bias lowers the threshold voltage of transistor 310 and transistor 320, and increases the off state current of transistor 310 and 320. Thus, additional leakage current from transistor 320 can compensate for the current loss at storage node 2 in order to maintain the logic high state.

[0027] While operating in the READ mode, both bit lines are at a high logic level, while WORDLINE is at a low logic level. Assuming that storage node 1 starts at a low logic level and storage node 2 starts at a high logic level, storage

node 1 is driven high and storage node 2 is driven low. Consequently, current will flow through transistor 310 from BITLINE to storage node 1. As described above, the body control signal is received at transistors 310 and 320 as a reverse bias during the READ mode.

[0028]   Reverse bias is a voltage supplied to transistors 310 and 320 that is greater than Vcc. The reverse bias makes transistors 310 and 320 increases the threshold voltage of transistor 310 and the ratio of the drive current of NMOS over PMOS transistors increases. As a result, storage node 1 is prevented from being pulled up during the read by current from transistor 310, causing the memory cell to flip. Thus, the read stability of memory cell 300 is improved.

[0029]   **Figure 4** illustrates one embodiment of a memory 400. According to one embodiment, memory 400 is implemented as cache 102. However, memory 400 may be implemented as any type of SRAM device used in computer system 100. Memory 400 includes memory cells 410, N-well 415, gap cell 420, N-well contact 430 and a control signal 440.

[0030]   Memory cells 410 include a PMOS component (e.g., transistors 310 and 320) and a NMOS component (e.g., transistors 330 and 340). N-well 415 includes the network of p-channel transistors formed within. Thus, all PMOS components in each memory cell 410 of memory 400 share N-well 415. Gap cell 420 in memory 400 that is used for wordline strapping.

[0031]   N-well contact 430 is located within gap cell 420. A control signal 440 is coupled to contact 430. in gap 420. Control signal 440 is a body control

signal that is delivered to contact 430. Thus, each PMOS component within memory 400 receives body control 440. As described above, control signal 440 delivers bias voltages to the PMOS component of memory cells 410. By routing control signal 440 from N-well contact 430, the area impact from transistors 330 and 340 is minimized.

[0032]   The delivery of bias signals to 4T memory cells, enable smaller transistors to be implemented within the cells. As a result, the 4T memory cells are operable with an even smaller area, resulting in smaller SRAMs.

[0033]   Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims which in themselves recite only those features regarded as the invention.

[0034]   Thus, a biasing technique for SRAMs implementing four transistor memory cells has been described.